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Russell Marc Kobert, Examiner	U.S. Patent and Trademark 703-308-5222 Office		703-308-7724	
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DATE:	October 28, 2002		Reviewed and approved	
FROM:	Morgan S. Heller II		for facsimile	
OPERATOR:	Karen S. Jeffer		transmission by:	
CLIENT/MATTER:	02016-00115		MSL	

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Comments

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Cook et al.

Serial No.: 09/751,355

Filed: December 28, 2000

Title: System and Method of Testing a

Microelectronic Device Using a

Duel Probe Technique

Attorney Docket No.: 02016-00115

Group Art Unit: 2829

Examiner: Russell Marc Kobert

Box Non-Fee Amendment

Commissioner for Patents Washington, DC 20231

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Morgan S Holler II

Date

October 28, 2002

Response Transmittal

Transmitted herewith for filing is an Amendment and Response to the above-identified Application.

No additional fee is required.

The fee has been calculated as shown below:

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P248-12/00

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CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
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INDEPENDENT 2	MINUS	2	=	x \$84.00/ \$42.00 =	\$.00
IST PRESENTATION OF MULTIPLE DEP. CLAIMS			\$280.00/ \$140.00 =	\$.00	
1				TOTAL	\$.00

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Respectfully submitted,

OCT 282002

DOWNS RACHLIN MARTIN PILICY CENTER 2800

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BTV/227529.1

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(02016-00115)

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RESPONSE TO FIRST OFFICE ACTION

This is in response to the Office Action (paper no. 4) mailed from the United States Patent and Trademark Office on July 29, 2002, with respect the above-identified application.

AMENDMENT

Please amend the application, without prejudice, as follows:

In the Specification:

Substitute the following paragraphs for the corresponding existing paragraphs. Markedup versions of these paragraphs showing the amendments made appear in an attachment hereto.

At page 1, line 10 to page 2, line 10, the first three paragraphs of the section entitled "BACKGROUND OF THE INVENTION":

As manufacturers continually reduce the size of microelectronic devices contained in very large scale integration (VLSI) integrated circuits (ICs), it is becoming more difficult